

REMARKS

Claims 1 and 8 have been amended. Claims 16-20 have been added. Thus, Claims 1-20 are pending in the present application.

Claim rejection under 35 USC §102(b):

The Examiner rejected claims 1-15 under 35 USC §102(e) as being anticipated by Fields. The Examiner stated that Fields discloses all the limitations of the independent claims. Applicant respectfully disagrees. However, to further prosecution Applicant amended independent claims 1 and 8. The independent claims of the present invention comprise limitations neither disclosed nor suggested by Fields.

Fields discloses a multi-processor system in Fig. 3 which uses a plurality of interconnected processors. These processors are part of a single system which runs a single operating system supporting multiple processors. Furthermore, according to Fig. 3 and the associated description in paragraphs [0024] - [0030], the system discloses provides for a common service processor which is coupled with the rest of the multi-processor system through a bus 347 that is controlled only by bus controllers 345 and 346. However, these controllers only establish a connection to a single processor or to a single system comprising multiple processors.

The present invention as defined in the independent claims, however, concerns a computer system with a plurality of independent sub-computer systems. According to the specification of the present application, a sub-computer system is a single personal computer or a single server. See page 6, line 4-6. In particular independent claims 8 and 13 emphasize this interpretation because they include the further limitation that each sub-system runs its own operating system. Applicant amended claims 1 and 8 to more clearly define this limitation. Each sub-system includes furthermore a link to the management controller through a serial interface output of a buffer device that is connected to a serial interface of the sub-computer system.

Fields does not show such an arrangement. The interconnected processors 310 are not independent sub-computer systems. Furthermore, according to Fig. 3 and the associated description of Fields, only a single RIO Bus Controller 346 is coupled with the management unit

340. Furthermore, Fields is silent as to what is included in a RIO Bus Controller. Thus, it is not clear whether such a controller includes any type of buffer as required by the independent claims.

With respect to dependent claim 2 and 11, the Examiner states that Fields discloses a microcontroller having a memory, a serial input a memory and a serial output and a switch coupled to the serial output. Applicant respectfully disagrees. None of these elements is disclosed by Fields. The Examiner states that the communication controller is formed by the I/O controller 352. However, the I/O controller 352 is part of the management controller and not part of any sub-system. Furthermore, the I/O controller 352 is not connected to any component of the system but rather provides an interface for external keyboard, mouse, serial interfaces, etc which are all external parts of the system which have nothing to do with the retrieval of crash dump data.

With respect to claim 3, 4, and 15 the Examiner asserts that Fields discloses that the serial output is part of a RS232 serial interface, USB and serial bus. Applicant respectfully disagrees. The Examiner refers to page 2, paragraph [0021] which relates to Fig. 2. Fig. 2, however, merely shows a single computer system. With respect to Fig. 3, to which all other citations of the Examiner refer, the only connection of the management controller to the multi-processors is shown by RIO Bus 347. This bus is however clearly not an RS232 or USB serial interface.

With respect to claim 5 and 12, Fig. 4 only shows a single connection to RIO Bus Controller 346. The description is silent with respect to all other RIO Controllers. Moreover, these controllers are clearly not coupled with the management unit 340.

With respect to the remaining dependent claims include all the limitations of the respective independent claims to which they refer. Thus these claims are at least patentable to the extent of the respective independent claims.

CONCLUSION

The application as defined in the pending claims is patentable under 35 U.S.C. §102 and §103 in view of the cited prior art. Therefore, applicants respectfully request withdrawal of the rejection and allowance of all pending claims.

Applicants do not believe that any other fees are due at this time; however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason relating to this document, the Commissioner is authorized to deduct the fees from Deposit Account No. 02-0383, (*formerly Baker & Botts, L.L.P.*,) Order Number 016295.0748.

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